

# BID DOCUMENT

## NATIONAL COMPETITIVE BIDDING

### FOR

SUPPLY, INSTALLATION, COMMISSIONING & MAINTENANCE OF EQUIPMENTS  
FOR  
COMPUTER SCIENCE ENGINEERING LABORATORY AT I.K.G.PTU KAPURTHALA  
AND ITS OTHER CONSTITUENT CAMPUSES (PUNJAB)

**Bid No. :** EdCIL/PROC/PTU-2017/LAB-BTECH-CSE/CSE-PKG1/1

## PART-II- FINANCIAL BID



### EdCIL (India) Limited

*(A Govt. of India Mini Ratna Enterprises)*

'EdCIL House', Plot No. 18A, Sector- 16A

NOIDA – 201301 (UP), INDIA

Tel: 0120 – 2512001-006, FAX: 0120-2515372

Dated: 06.05.2017

This document serially numbered from page number 01 to 19.

**FINANCIAL BID**  
**Instructions to Bidders**

1. Financial Bid shall be submitted with full price details.

Financial Bid shall contain only the prices duly filled in as per the format given in Schedule of Rates provided in the tender document. Price bid should not have any Commercial and/or Technical stipulation in addition to, what is already given in Part I – Technical bid.

Financial Bid Standard Forms (Form-1, Form-2A and /or Form-2B) shall be used for the preparation of the price quote according to the instructions provided.

2. **The Bidder should quote for all the Laboratory items / equipments listed in this document. In case, the Bidder/s does not quote for all the Laboratory items/Equipments, the Bid shall be treated as incomplete and shall be rejected summarily.**
3. The Items / equipments to be supplied / delivered / installed / commissioned at various locations of IKGPTU Campuses is as shown in the enclosed Annexure VI. The rate shall be inclusive of all taxes, octroi, transportation (as per the location), packing, loading and unloading (as designated location), Insurance etc. and nothing shall be paid extra.
4. The bid shall be evaluated on total value of all Laboratory items/Equipments as shown in summary and supply order shall be placed to a bidder as a composite bid.
5. The prices quoted by the bidder shall be fixed for the quantity mentioned for the duration of the contract and shall not be subject to adjustment on any account. Price should be firm for any positive or negative variation in quantities up to 100%.
6. The changes displayed in the corrigendum/addendum to the bid documents, particularly with the financial bid should be attached with the financial bid submission, in the same packet, duly signed and stamped by the authorized signatory of the Bidder firm.

**FINANCIAL BID SUBMISSION FORM**

To:

Chief General Manager (EIS & EPS)  
EdCIL (India) Limited  
EdCIL House, 18 A, Sector-16 A  
NOIDA – 201301 (U.P.), India

Dated: \_\_\_\_/\_\_\_\_/2017

Dear Sir,

We, the undersigned, offer to provide "SUPPLY, INSTALLATION , COMMISSIONING & MAINTENANCE OF LABORATORY EQUIPMENTS" in accordance with your Request for Proposal dated \_\_\_\_/\_\_\_\_/2017.

Our attached Financial Bid is for the amount of \_\_\_\_\_ *[Indicate the corresponding to the amount(s), currency(ies) {Insert amount(s) in words and figures}]*.

Please note that all amounts shall be the same as in Form-1. Our Financial Bid shall be binding upon by us subject to the modifications resulting from Contract negotiations, if any, up to expiration of the validity period of the Proposal.

We remain,

Yours sincerely,

Authorized Signature {In full and initials}:

Name and Title of Signatory:

In the capacity of:

Address:

E-mail:

**FORM-1****SUMMARY OF FINANCIAL BID**

S. No.	Description	Amount (exclusive of Tax) (Rs.)	Tax (Rs.)	Amount (Inclusive of Tax) (Rs.)
A.	COMPUTER SCIENCE ENGINEERING LABORATORY EQUIPMENTS (Form- 2A and/or Form-2B)			
B.	Comprehensive Annual Maintenance (Annexure-IV)			
	<b>Total (Rs.)</b>			
Total Price Bid (exclusive of taxes) (in Words)				
(Rupees.....)				
Total Price of Bid (Inclusive of taxes) (In Words)				
(Rupees.....)				
Signature of bidder		.....		
Name & Address		..... ..... .....		
Note :	Date		.....	
i)	<i>Discount or any other offers affecting the package price must be mentioned here only. Discount or any other offers affecting the package price mentioned at any other place of the bid will not be considered.</i>			
ii)	<i>In case of discrepancy between unit price and total price, the unit price shall prevail.</i>			
iii)	<i>Bids shall be evaluated based on total price without taxes.</i>			

**FORM-2A**  
**(FINANCIAL BID)**

**PRICE SCHEDULED FOR GOODS TO BE IMPORTED FROM ABROAD**

**ANNEXURE – I**  
**Date: .....**

**Name of the Department:**

**Name of the Laboratory:**

**(A) Price Schedule: (Format used for imported items)**

S.No.	Currency	Description and Specification of the Item	Qty. in Units	Unit Price	Agency Commission (If applicable)	Discount	Ex-works price	Packing + Handling + DOC + Inland Freight	FOB price	Insurance + Freight	CIF Price	Total Price
			(a)	(b)	(c)	(d)	(e)=(b+c-d)	(f)	(g)=(e+f)	(h)	(i) = (g+h)	(j) = (i*a)
	INR			(i)In Figures: (ii)In words:								

**Total Price of Bid (In Words) .....**

**Signature of bidder** .....

**Name & Address** .....

**Date** .....

**Note:**

- The above financial template should be strictly followed. Any deviation from the above template (in terms of description and specification of the item) may debar the bidder at sole discretion of EdCIL.*
- Discount or any other offers affecting the package price must be mentioned here only. Discount or any other offers affecting the package price mentioned at any other place of the bid will not be considered.*
- In case of discrepancy between unit price and total price, the unit price shall prevail.*
- Bids shall be evaluated based on total price including all charges as CIF Price.*

## FORM-2B

## ANNEXURE-II

**PRICE SCHEDULED FOR INDIGENOUS GOODS****Price Schedule: (Format used for indigenous items).**

S.No.	Description and Specification of the Item	Qty. in Units	Unit Price in Rs.	Excise Duty %	CST/ VAT %	Insurance other duties and taxes if any,	Packing and Inland Transportat ion	CIF Price	Total Price in Rs. (Excluding Taxes)	Total Price in Rs. (Including Taxes)
		(a)	(b)	(c)	(d)	(e)	(f)	(g)	(h)=(b*a)	(i) = (g *a)
			(i)In Figures: (ii)In words:							
<b>Total Price of Bid (In Words)</b> .....										
<b>Signature of bidder</b>						.....				
<b>Name &amp; Address</b>						.....				
<b>Date</b>						.....				
<b>Note:</b> <ol style="list-style-type: none"> <li><i>The above financial template should be strictly followed. Any deviation from the above template (in terms of description and specification of the item) may debar the bidder at sole discretion of EdCIL.</i></li> <li><i>Discount or any other offers affecting the package price must be mentioned here only. Discount or any other offers affecting the package price mentioned at any other place of the bid will not be considered.</i></li> <li><i>In case of discrepancy between unit price and total price, the unit price shall prevail.</i></li> <li><i>Bids shall be evaluated based on total price including all charges as CIF Price.</i></li> </ol>										

**ANNEXURE – III**

**COMPREHENSIVE ANNUAL MAINTENANCE CONTRACT PRICES SCHEDULE**

S. No.	Item Description	2 <sup>nd</sup> Yr.	3 <sup>rd</sup> Yr.	Total Comprehensive Annual Maintenance Contract for 2 years(2 <sup>nd</sup> year & 3 <sup>rd</sup> year) after warranty period of 1 year from the date of successful installation. (E= C+D)
A	B	C	D	E
1.	Equipment: Make: Model: Qty.: (Mention Total quantity from Annexure-VI)			
<b>SUB-TOTAL(Rs.)</b> (Carry forwarded to Summary)				
<b>Sub-Total Price Bid (exclusive of taxes) (in Words)</b> (Rupees.....)				
<b>Sub-Total Price of Bid (Inclusive of taxes) (In Words)</b> (Rupees.....)				
Signature of bidder		.....		
Name & Address		..... .....		
<b>Note:</b>	Date		.....	
i)	<b><i>Discount or any other offers affecting the package price must be mentioned here only. Discount or any other offers affecting the package price mentioned at any other place of the bid will not be considered.</i></b>			
ii)	<b><i>In case of discrepancy between unit price and total price, the unit price shall prevail.</i></b>			
iii)	<b><i>Bids shall be evaluated based on total price without taxes.</i></b>			

**Note:**

- The above rates shall be included in computing the total cost of the equipments.***
- Agency to use separate sheet for each equipment/Item/package.***

**DETAILED TECHNICAL SPECIFICATIONS:****ANNEXURE-IV**

<b>Sr. No.</b>	<b>Name of Items</b>	
1	<b>Digital IC Trainer</b>	<p><b>Full System: (Gates, FF'S, counters)</b></p> <ul style="list-style-type: none"> <li>❖ +5V / 1 Amp DC power Supply</li> <li>❖ Quad 2-Input NAND Gate (7400)</li> <li>❖ Quad 2-Input NOR Gate (7402)</li> <li>❖ Quad 2-Input AND Gate (7408)</li> <li>❖ Quad 2-Input OR Gate (7432)</li> <li>❖ Hex Inverters (7404)</li> <li>❖ Dual 4-Input NAND Gate (7420)</li> <li>❖ Dual 4-Input NOR Gate (7425)</li> <li>❖ Dual 2-Ex-OR Gate (7486)</li> <li>❖ Dual JK Flip Flop (7476)</li> <li>❖ 4-Bit R /L Shift Register (7495)</li> <li>❖ Up / Down Binary Counter (74193)</li> <li>❖ 4-Bit Binary Full Adder (7483)</li> <li>❖ 4-Bit Magnitude Comparator (7485)</li> <li>❖ BCD to 7-Segment Decoder (7447)</li> <li>❖ Monostable Multivibrator (74121)</li> <li>❖ Synchronous Binary Counter (74163)</li> <li>❖ Decade Counter (7490)</li> <li>❖ 7-Segment LED Display (2 Nos.)</li> <li>❖ Logic Input Switches (10 Nos.)</li> <li>❖ Logic Status Indicators (10 Nos.)</li> <li>❖ Bounce less Pulsar</li> <li>❖ 1Hz &amp; 1KHz TTL Clocks</li> <li>❖ Assembled in standard material Box.</li> </ul> <p>Set of patch Chords &amp; Experimental Manual</p>
2	<b>Half &amp; Full Adder &amp; Sub tractor</b>	<ul style="list-style-type: none"> <li>❖ XOR Gate three input (1 Nos.)</li> <li>❖ NOT Gates (3 Nos.)</li> <li>❖ Logic I/P Switches, (3 Nos.)</li> <li>❖ Status Indicators LED, (4 Nos.)</li> <li>❖ +5 V/350mA DC Power Supply,</li> <li>❖ Assembled in standard material Box.</li> </ul> <p><u>Set of Patch Chords &amp; Experimental Manual.</u></p>



3	<b>Half &amp; Full Adder &amp; Sub tractor</b>	<ul style="list-style-type: none"> <li>❖ NAND Gates (7400), (2 Nos.)</li> <li>❖ NOT Gate (1 Nos.)</li> <li>❖ Logic I/P Switches, (3 Nos.)</li> <li>❖ Status Indicators LED, (4 Nos.)</li> <li>❖ +5 V/350mA DC Power Supply,</li> <li>❖ Assembled in standard material Box.</li> <li>❖ Set of Patch Chords &amp; Experimental Manual.</li> </ul>
4	<b>4-Bit Binary to Gray &amp; Gray to Binary Converter</b>	<ul style="list-style-type: none"> <li>❖ Built in +5V / 350mA Fixed DC Voltage Source,</li> <li>❖ Logic Input Switches, (4 Nos.)</li> <li>❖ Logic Status Indicators, (4 Nos.)</li> <li>❖ Ex-OR Gates, (3 Nos.)</li> <li>❖ 4-Bit Binary to Gray &amp; Gray to Binary Converter</li> <li>❖ Assembled in standard material Box.</li> <li>❖ Set of patch Chords &amp; Experimental Manual.</li> </ul>
5	<b>4-bit and 8-Bit Magnitude Comparator</b>	<ul style="list-style-type: none"> <li>❖ 4-Bit Magnitude Comparator (7485),</li> <li>❖ Logic I / P Switches, (11 Nos.)</li> <li>❖ Logic Status Indicators, (3 Nos.)</li> <li>❖ +5V / 350mA DC Power Supply,</li> <li>❖ Assembled in standard material Box.</li> <li>❖ Set of Path Chords &amp; Experimental Manual.</li> </ul>
6	<b>8-Line to 1-Line Multiplexer &amp; Demultiplexer</b>	<ul style="list-style-type: none"> <li>❖ 8-Line to 1-Line Multiplexer, (74151/74153)</li> <li>❖ Address Generator, (7493)</li> <li>❖ 1 K Hz TTL Clock,</li> <li>❖ Logic I / P Switches, (3Nos.)</li> <li>❖ Logic Status Indicator (1Nos.)</li> <li>❖ +5V/ 350mA DC Power Supply,</li> <li>❖ Assembled in standard material Box</li> <li>❖ Set of Patch Chords &amp; Experimental Manual</li> </ul>
8	<b>RS, D, T &amp; JK Flip Flops</b>	<ul style="list-style-type: none"> <li>❖ RS, D &amp; T Flip Flops one each using (IC 7400, 7447,7476)</li> <li>❖ Logic I / P Switches (4 Nos.)</li> <li>❖ Logic Status Indicators, (4 Nos.)</li> <li>❖ Bounce less Pulsar</li> <li>❖ +5V / 350mA DC Power Supply,</li> <li>❖ Assembled in standard material Box.</li> <li>❖ Set of Patch Chords &amp; Experimental Manual.</li> </ul>

9	<b>4-Bit Asynchronous Binary Counter</b>	<ul style="list-style-type: none"> <li>❖ 4 –bit up counter and Mod-N counter using IC 7490 and IC 7493 chip ,</li> <li>❖ Logic I/P Switches, (6 Nos.)</li> <li>❖ Logic Status Indicators, (4 Nos.)</li> <li>❖ 1 Hz &amp; 1KHz TTL clock,</li> <li>❖ +5 V/350 mA. DC Power Supply,</li> <li>❖ Assembled in standard material Box.</li> <li>❖ Set of Patch Chords &amp; Experimental Manual.</li> </ul>
10	<b>4-Bit Synchronous Binary Counter</b>	<ul style="list-style-type: none"> <li>❖ 4 –bit up/down counter and Mod-N counter using IC 74192 and IC 74193 chip,</li> <li>❖ Logic I/P Switches, (6 Nos.)</li> <li>❖ Logic Status Indicators, (4 Nos.)</li> <li>❖ 1 Hz &amp; 1KHz TTL clock,</li> <li>❖ +5 V/350 mA. DC Power Supply,</li> <li>❖ Assembled in standard material Box.</li> <li>❖ Set of Patch Chords &amp; Experimental Manual.</li> </ul>
11	<b>Shift Registers-SISO, SIPO, PISO, PIPO</b>	<ul style="list-style-type: none"> <li>❖ SISO (7491), SIPO (74164), PISO (74165), PIPO (74194/7495),</li> <li>❖ Logic Status Indicators, (16Nos.)</li> <li>❖ 1 Hz &amp; 10 Hz TTL Clocks,</li> <li>❖ +5V / 350mA DC Power Supply,</li> <li>❖ Assembled in standard material Box.</li> <li>❖ Set of Patch Chords &amp; Experimental Manual.</li> </ul>
12	<b>8-Bit Digital to Analog Converter (DAC)</b>	<ul style="list-style-type: none"> <li>❖ 8-Bit Digital to Analog Converter using DAC(IC 0800 chip), obtain staircase waveform using DAC.</li> <li>❖ 1 K Hz TTL Clock,</li> <li>❖ Logic Input Switches, (8 Nos.)</li> <li>❖ Logic Status Indicators, (8 Nos.)</li> <li>❖ +5V &amp; +12V / 350mA DC Power Supply,</li> <li>❖ Assembled in standard material Box.</li> <li>❖ Set of Patch Chords &amp; Experimental Manual.</li> </ul>
13	<b>8-Bit Analog to Digital Converter (ADC)</b>	<ul style="list-style-type: none"> <li>❖ Analog to Digital Converter</li> <li>1) Successive approximation Using ADC (0809)</li> <li>❖ 1 K Hz TTL Clock,</li> <li>❖ Logic Status Indicators, (16Nos.)</li> <li>❖ 0 to 5V Variable Analog Signal,</li> <li>❖ +5V &amp; +/-12V / 350mA DC Power Supply,</li> <li>❖ Assembled in standard material Box.</li> <li>❖ Set of Patch Chords &amp; Experimental Manual.</li> </ul>

14	<b>8085 MICROPROCESSOR TRAINER KIT</b>	<p><b><u>Specification:-</u></b></p> <p>8085 Microprocessor CPU. MEMORY CAPACITY:</p> <ol style="list-style-type: none"> <li>1. 4KB SCRATCH PAD RAM, 16 KB BATTERY-BACKUP RAM (with onboard Ni-Cd rechargeable Battery),</li> <li>2. 36KB EPROM Monitor With Advance Softwares Like One-Pass Line Assembler, Two Pass Assembler &amp; Dis-Assembler, Hex Dump.</li> </ol> <ul style="list-style-type: none"> <li>• ONBOARD 8251, 8253, 8255 (2 Nos.), 8259</li> <li>• Should support 101 keys PC AT keyboard.</li> <li>• Should consist of ONBOARD PC/AT KEYBOARD INTERFACE with necessary socket for connecting PC keyboard.</li> <li>• Should consist of a 20 CHARACTER x 4 LINES Bright, Back-lit L.C.D.</li> <li>• Uploading &amp; Downloading facility from PC.</li> </ul>
15	<b>8086 MICROPROCESSOR TRAINER KIT</b>	<p>8086 Microprocessor CPU.</p> <ul style="list-style-type: none"> <li>• MEMORY CAPACITY: <ol style="list-style-type: none"> <li>1. 64KB SCRATCH PAD RAM, 64 KB BATTERY-BACKUP RAM (with onboard Ni-Cd rechargeable Battery),</li> <li>2. 128 KB Eprom.</li> </ol> </li> <li>• ONBOARD 8251, 8253, 8255 (2 Nos.), 8259, &amp;</li> <li>• Should support 101 keys PC AT keyboard.</li> <li>• Should consist of a 16 x 2 CHARACTER Back-lit L.C.D.</li> <li>• Uploading &amp; Downloading facility from PC.</li> </ul>
16	<b>Motor Drive Module</b>	<p><b>Stepper Motor</b> : +5 V</p> <p><b>DC Motor</b> : +12 V</p> <p><b>Servo Motor</b> : +5 V</p> <p><b>Interface</b> : 20 pin FRC cable</p> <p><b>Test points</b> : 13 (Gold plated)</p>

17	<b>Display Interfacing module</b>	Scanning techniques 8x8 LED Matrix, 4x4 keypad 7 segment 8 digit LED display.
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## ANNEXURE-V

## TECHNICAL COMPLIANCE REPORT:

## A. Laboratory Equipments

Sr. No.	Name of Items	Numerical Values and Other information	Whether Comply (Yes/No)
1	<b>Digital IC Trainer</b> Full System: (Gates, FF'S, counters) ❖ +5V / 1 Amp DC power Supply		
	❖ Quad 2-Input NAND Gate (7400)		
	❖ Quad 2-Input NOR Gate (7402)		
	❖ Quad 2-Input AND Gate (7408)		
	❖ Quad 2-Input OR Gate (7432)		
	❖ Hex Inverters (7404)		
	❖ Dual 4-Input NAND Gate (7420)		
	❖ Dual 4-Input NOR Gate (7425)		
	❖ Dual 2-Ex-OR Gate (7486)		
	❖ Dual JK Flip Flop (7476)		
	❖ 4-Bit R /L Shift Register (7495)		
	❖ Up / Down Binary Counter (74193)		
	❖ 4-Bit Binary Full Adder (7483)		
	❖ 4-Bit Magnitude Comparator (7485)		
	❖ BCD to 7-Segment Decoder (7447)		
	❖ Monostable Multivibrator (74121)		
	❖ Synchronous Binary Counter (74163)		
	❖ Decade Counter (7490)		
	❖ 7-Segment LED Display (2 Nos.)		
	❖ Logic Input Switches (10 Nos.)		
	❖ Logic Status Indicators (10 Nos.)		
	❖ Bounce less Pulsar		
	❖ 1Hz & 1KHz TTL Clocks		
	❖ Assembled in standard material Box.		
	❖ Set of patch Chords & Experimental Manual.		
2	<b>Half &amp; Full Adder &amp; Sub tractor</b> ❖ XOR Gate three input (1 Nos.)		
	❖ NOT Gates (3 Nos.)		
	❖ Logic I/P Switches, (3 Nos.)		
	❖ Status Indicators LED, (4 Nos.)		
	❖ +5 V/350mA DC Power Supply, ❖ Assembled in standard material Box.		

	❖ Set of Patch Chords & Experimental Manual.		
3	<b><u>Half &amp; Full Adder &amp; Sub tractor</u></b> ❖ NAND Gates (7400),  ❖ NOT Gate (1 Nos.) ❖ Logic I/P Switches, (3 Nos.) ❖ Status Indicators LED, (4 Nos.) ❖ +5 V/350mA DC Power Supply, ❖ Assembled in standard material Box. ❖ Set of Patch Chords & Experimental Manual.		
4	<b>4-Bit Binary to Gray &amp; Gray to Binary Converter</b> ❖ Built in +5V / 350mA Fixed DC Voltage Source, ❖ Logic Input Switches, (4 Nos.) ❖ Logic Status Indicators, (4 Nos.) ❖ Ex-OR Gates, (3 Nos.) ❖ 4-Bit Binary to Gray & Gray to Binary Converter ❖ Assembled in standard material Box. ❖ Set of patch Chords & Experimental Manual.		
5	<b>4-bit and 8-Bit Magnitude Comparator</b> ❖ 4-Bit Magnitude Comparator (7485), ❖ Logic I / P Switches, (11 Nos.) ❖ Logic Status Indicators, (3 Nos.) ❖ +5V / 350mA DC Power Supply, ❖ Assembled in standard material Box. ❖ Set of Path Chords & Experimental Manual.		
6	<b>8-Line to 1-Line Multiplexer &amp; Demultiplexer</b> ❖ 8-Line to 1-Line Multiplexer, (74151/74153) ❖ Address Generator, (7493) ❖ 1 K Hz TTL Clock, ❖ Logic I / P Switches, (3Nos.) ❖ Logic Status Indicator (1Nos.) ❖ +5V/ 350mA DC Power Supply, ❖ Assembled in standard material Box. ❖ Set of Path Chords & Experimental Manual.		
8	<b>RS, D T &amp; JK Flip Flops</b>  RS, D & T Flip Flops one each using (IC 7400, 7447,7476)		

	❖ Logic I / P Switches (4 Nos.)		
	❖ Logic Status Indicators, (4 Nos.)		
	❖ Bounce less Pulsar		
	❖ +5V / 350mA DC Power Supply,		
	❖ Assembled in standard material Box.		
	❖ Set of Patch Chords & Experimental Manual.		
9	<b>4-Bit Asynchronous Binary Counter</b> ❖ 4 –bit up counter and Mod-N counter using IC 7490 and IC 7493 chip ,		
	❖ Logic I/P Switches, (6 Nos.)		
	❖ Logic Status Indicators, (4 Nos.)		
	❖ 1 Hz & 1KHz TTL clock,		
	❖ +5 V/350 mA. DC Power Supply,		
	❖ Assembled in standard material Box.		
	❖ Set of Patch Chords & Experimental Manual.		
10	<b>4-Bit Synchronous Binary Counter</b> ❖ 4 –bit up/down counter and Mod-N counter using IC 74192 and IC 74193 chip,		
	❖ Logic I/P Switches, (6 Nos.)		
	❖ Logic Status Indicators, (4 Nos.)		
	❖ 1 Hz & 1KHz TTL clock,		
	❖ +5 V/350 mA. DC Power Supply,		
	❖ Assembled in standard material Box.		
	❖ Set of Patch Chords & Experimental Manual.		
11	<b><u>Shift Registers-SISO, SIPO, PISO, PIPO</u></b> ❖ SISO (7491), SIPO (74164), PISO (74165), PIPO (74194/7495),		
	❖ Logic Status Indicators, (16Nos.)		
	❖ 1 Hz & 10 Hz TTL Clocks,		
	❖ +5V / 350mA DC Power Supply,		
	❖ Assembled in standard material Box.		
	❖ Set of Patch Chords & Experimental Manual.		
12	<b>8-Bit Digital to Analog Converter (DAC)</b> ❖ 8-Bit Digital to Analog Converter using DAC(IC 0800 chip), obtain staircase waveform using DAC.		

	❖ 1 K Hz TTL Clock,		
	❖ Logic Input Switches, (8 Nos.)		
	❖ Logic Status Indicators, (8 Nos.)		
	❖ +5V & +12V / 350mA DC Power Supply,		
	❖ Assembled in standard material Box.		
	❖ Set of Patch Chords & Experimental Manual.		
13	<b>8-Bit Analog to Digital Converter (ADC)</b>  ❖ Analog to Digital Converter 1) Successive approximation Using ADC (0809)		
	❖ 1 K Hz TTL Clock,		
	❖ Logic Status Indicators, (16Nos.)		
	❖ 0 to 5V Variable Analog Signal,		
	❖ +5V & +/-12V / 350mA DC Power Supply,		
	❖ Assembled in standard material Box.		
	❖ Set of Patch Chords & Experimental Manual.		
14	<b>8085 MICROPROCESSOR TRAINER KIT</b>  <u><b>Specification:-</b></u>  8085 Microprocessor CPU. • MEMORY CAPACITY: <ol style="list-style-type: none"> <li>1. 4KB SCRATCH PAD RAM, 16 KB BATTERY-BACKUP RAM (with onboard Ni-Cd rechargeable Battery),</li> <li>2. 36KB EPROM Monitor With Advance Software Like One-Pass Line Assembler, Two Pass Assembler &amp; Dis-Assembler, Hex Dump.</li> </ol>		
	• ONBOARD 8251, 8253, 8255 (2 Nos.), 8259		
	• Should support 101 keys PC AT keyboard.		
	• Should consist of ONBOARD PC/AT KEYBOARD INTERFACE with necessary socket for connecting PC keyboard.		
	• Should consist of a 20 CHARACTER x 4 LINES		



	Brigt, Back-lit L.C.D.		
	<ul style="list-style-type: none"> <li>• Uploading &amp; downloading facility from PC.</li> </ul>		
15	<b>8086 MICROPROCESSOR TRAINER KIT</b>  8086 Microprocessor CPU. <ul style="list-style-type: none"> <li>• MEMORY CAPACITY: <ol style="list-style-type: none"> <li>1. 64KB SCRATCH PAD RAM, 64 KB BATTERY-BACKUP RAM (with onboard Ni-Cd rechargeable Battery),</li> <li>2. 128 KB Eprom.</li> </ol> </li> </ul>		
	<ul style="list-style-type: none"> <li>• ONBOARD 8251, 8253, 8255 (2 Nos.), 8259, &amp;</li> </ul>		
	<ul style="list-style-type: none"> <li>• Should support 101 keys PC AT keyboard.</li> </ul>		
	<ul style="list-style-type: none"> <li>• Should consist of a 16 x 2 CHARACTER Back-lit L.C.D.</li> </ul>		
	<ul style="list-style-type: none"> <li>• Uploading &amp; downloading facility from PC.</li> </ul>		
16.	<b>Motor Drive Module</b> <b>Stepper Motor : +5 V</b>		
	<b>DC Motor : +12 V</b>		
	<b>Servo Motor : +5 V</b>		
	<b>Interface : 20 pin FRC cable</b>		
	<b>Test points : 13 (Gold plated)</b>		
17.	<b>Display Interfacing module</b> Scanning techniques		
	8x8 LED Matrix,		
	4x4 keypad 7 segment 8 digit LED display.		

## ANEXURE-VI

## DETAILS OF EQUIPMENTS TO BE SUPPLIED AT VARIOUS IKGPTU CAMPUSES:

Sr. No	Name of Equipment	Kapurthala	Amritsar	Bhikhiwind	Dinanagar	Hoshiarpur	Total Quantity
1	Study of Logic gates truth table, verification of OR, AND, NOT, XOR, NAND and NOR gates; Realization of OR, AND, NOR and XOR functions using universal gates.	1	1	1	1	1	5
2	Half /Full Adder realization using basic and XOR gates	1	1	1	1	1	5
3	Half subtractor /Full subtractor realization using basic and NAND gates	1	1	1	1	1	5
4	4-Bit Binary to Gray & Gray to Binary Code Converter: Realization using XOR gates	1	1	1	1	1	5
5	4-bit and 8-Bit comparator : Implementation using IC 7485 magnitude comparator Chips	1	1	1	1	1	5
6	Multiplexer: Truth table verification and realization of full adder using IC 74153	1	1	1	1	1	5
7	Demultiplexer: Truth table verification and realization of Half subtractor and Full subtractor using IC 74139 chip	1	1	1	1	1	5
8	Flip Flops: Truth Table verification of JK master slave FF, T-type and D-Type F using IC7476 chip	1	1	1	1	1	5
9	Asynchronous Counter: Realization of 4 –bit up counter and Mod-N counter using IC 7490 and IC 7493 chip	1	1	1	1	1	5

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10	Synchronous Counter: Realization of 4 –bit up/down counter and Mod-N counter using IC 74192 and IC 74193 chip	1	1	1	1	1	5
11	Shift Register: Study of shift right, SIPO, PIPO, PISO and shift left operations using IC 7495 chip	1	1	1	1	1	5
12	DAC Operation: Study of 8-bit DAC(IC 08/0800 chip), obtain staircase waveform using IC 7495 chip	1	1	1	1	1	5
13	ADC operations: Study of 8-bit ADC	1	1	1	1	1	5
14	Introduction to 8085Kit: Addition, subtraction and Compliment of 8 bit numbers, Shift an 8 bit number by one bit, To find the largest of two 8 bit numbers Sum of series of 8 bit numbers	0	1	1	1	1	4
15	Introduction to 8086 kit Addition, Subtraction and compliment of 16 bit numbers	0	1	1	1	1	4
16	Motor Drive Module	0	1	1	1	1	4
17	Interfacing Display module	0	1	1	1	1	4